

FIG. 1 PRIOR ART

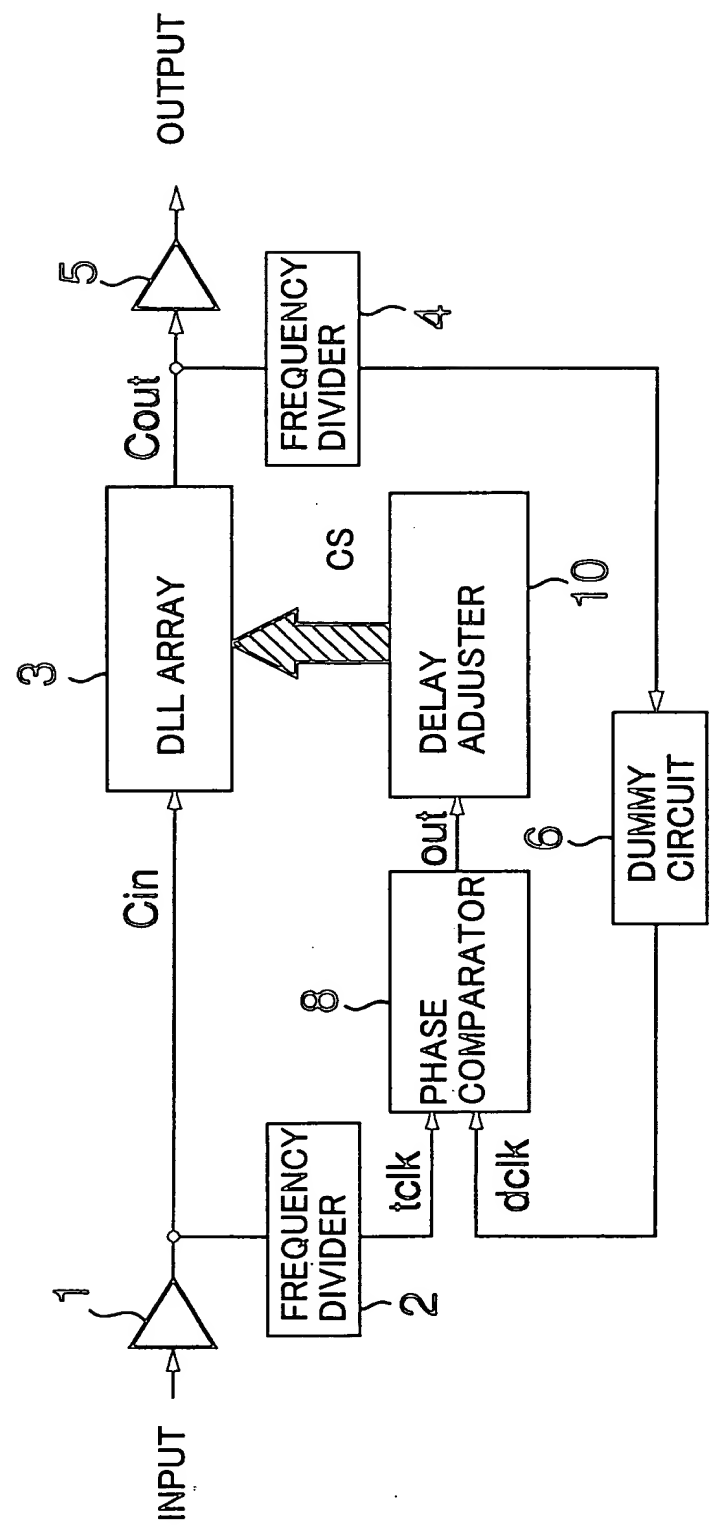
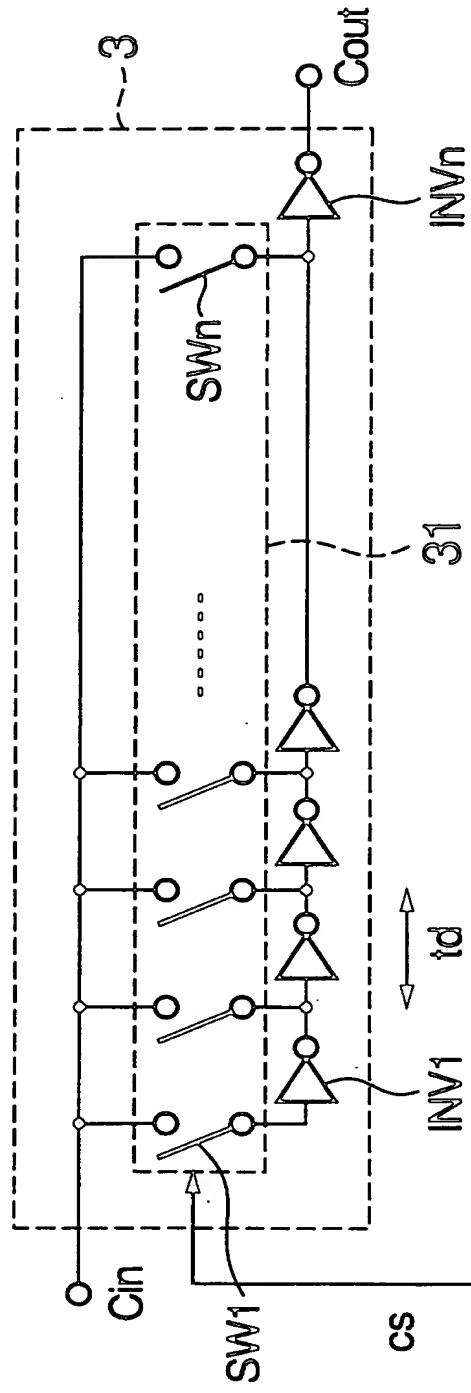
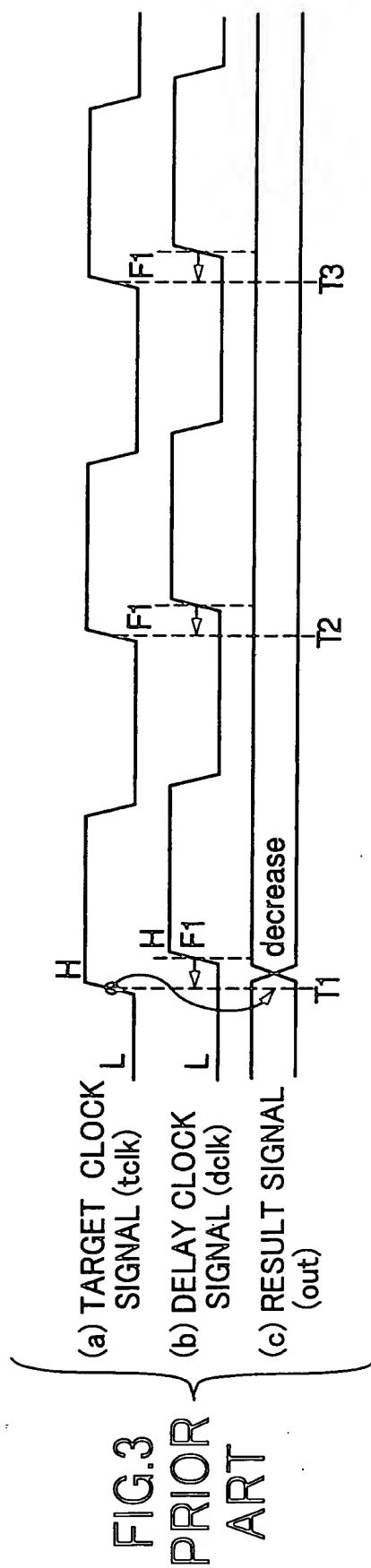
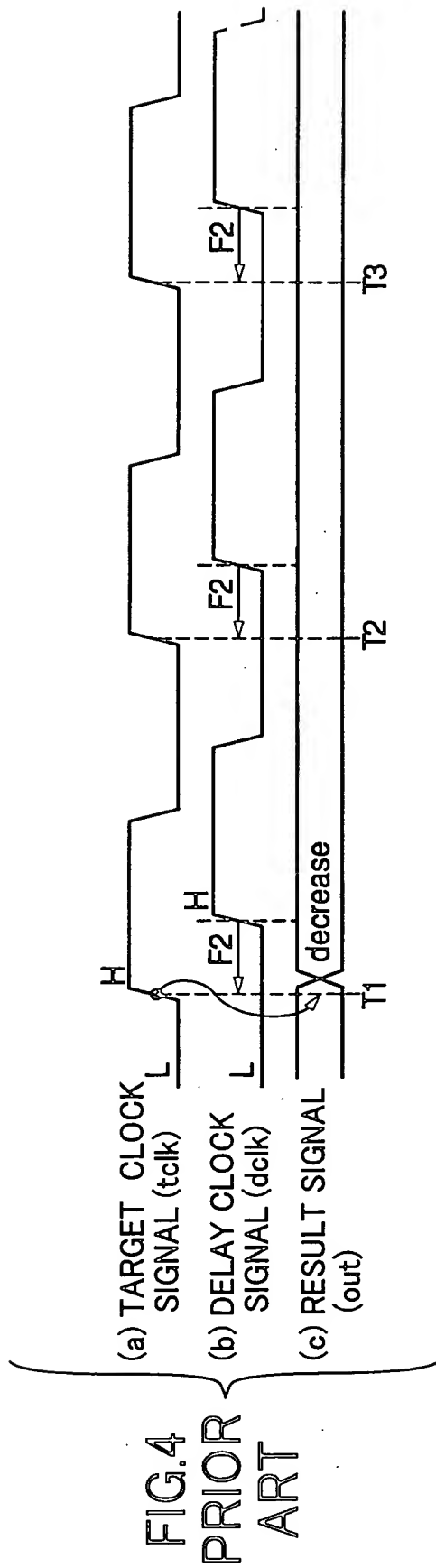
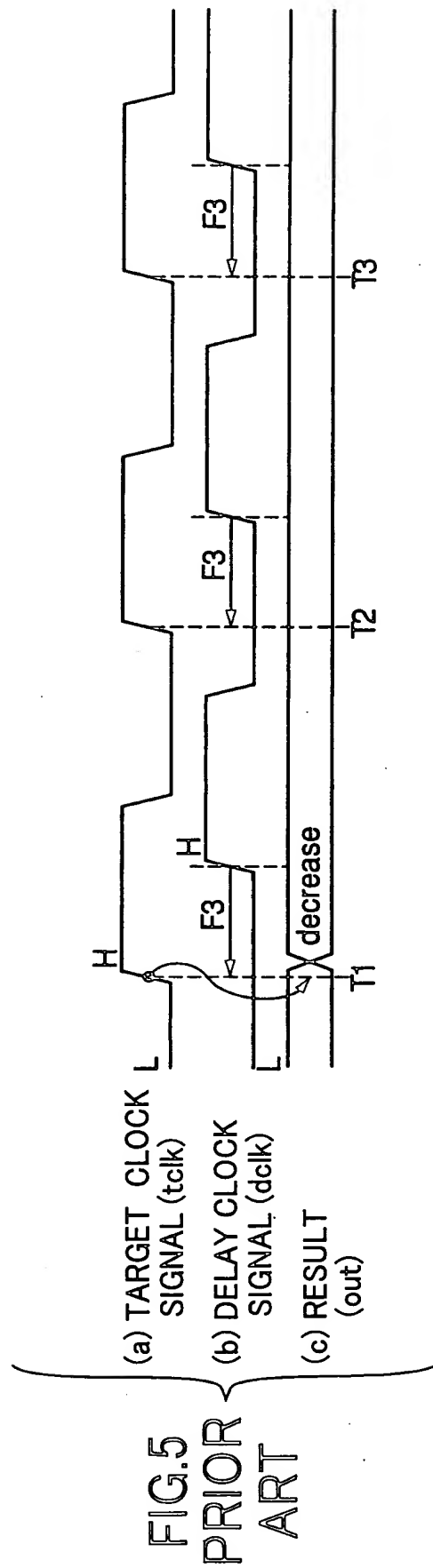


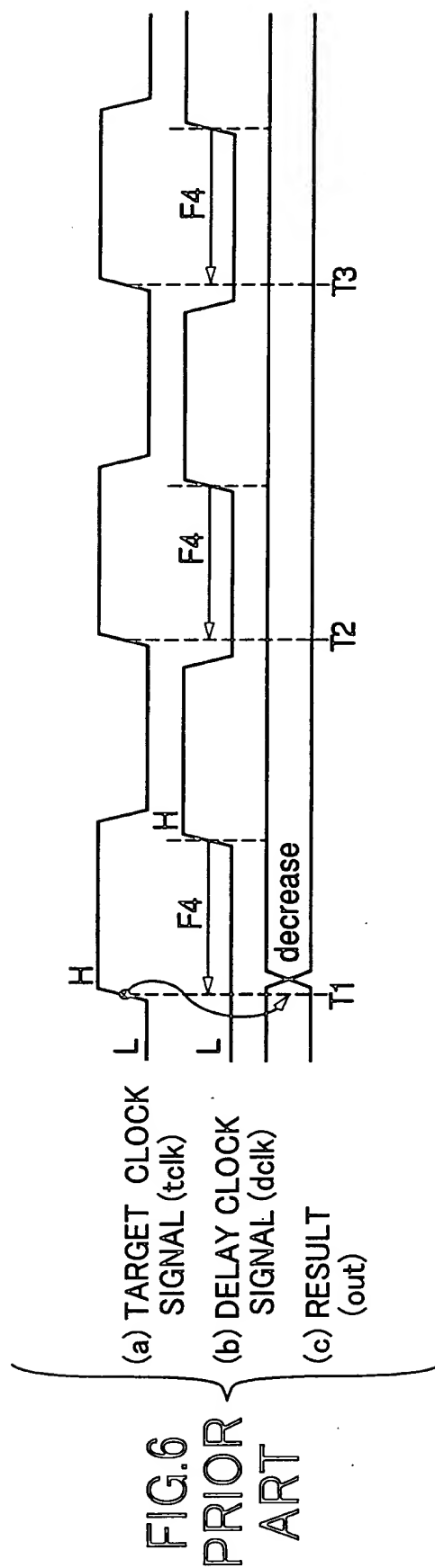
FIG. 2 PRIOT ART











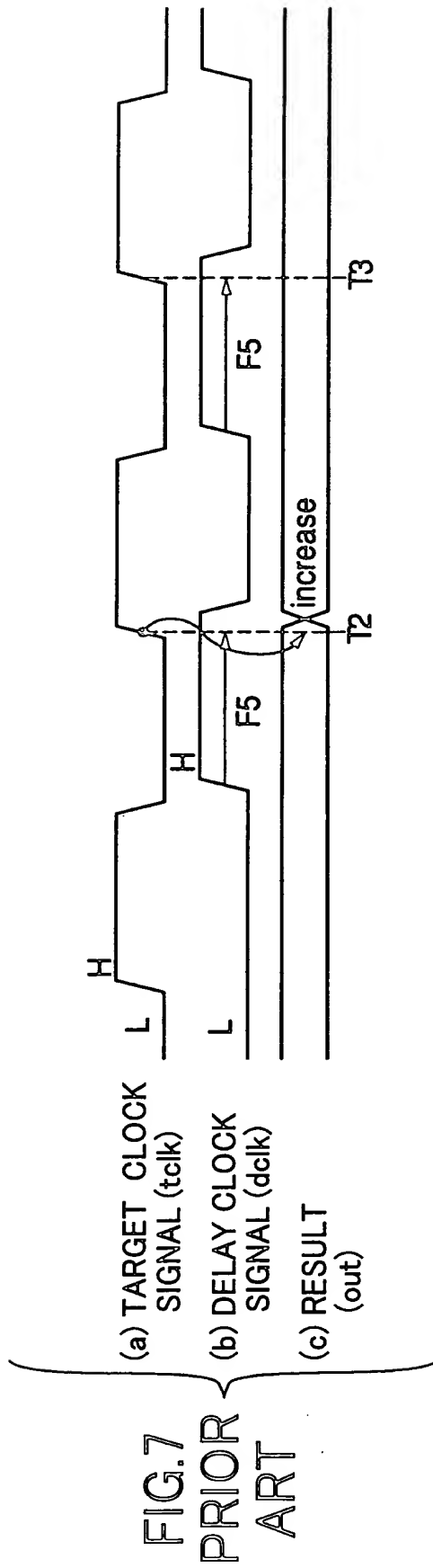


FIG. 8 PRIOR ART

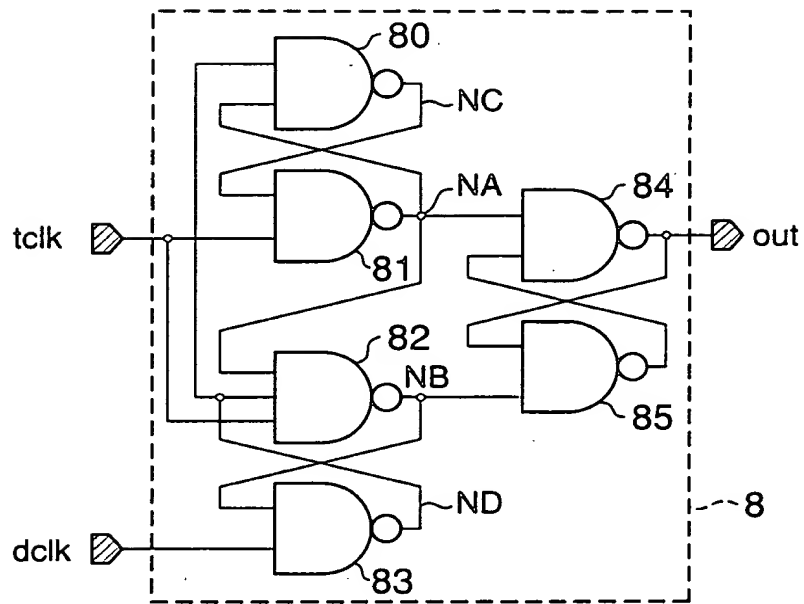


FIG. 8 PRIOR ART

FIG. 9
PRIOR
ART

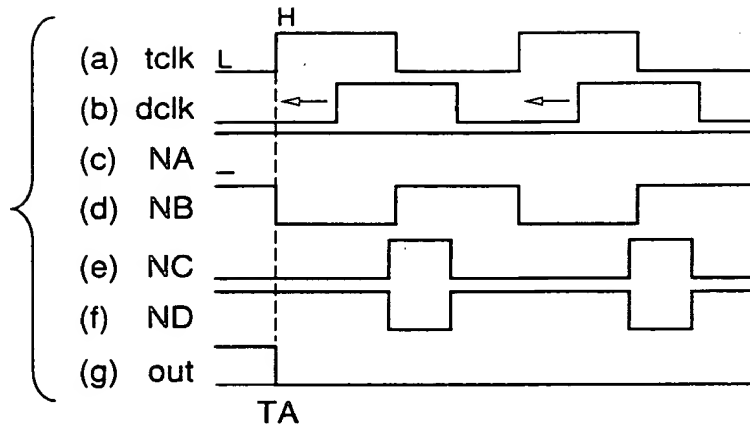


FIG. 10
PRIOR
ART

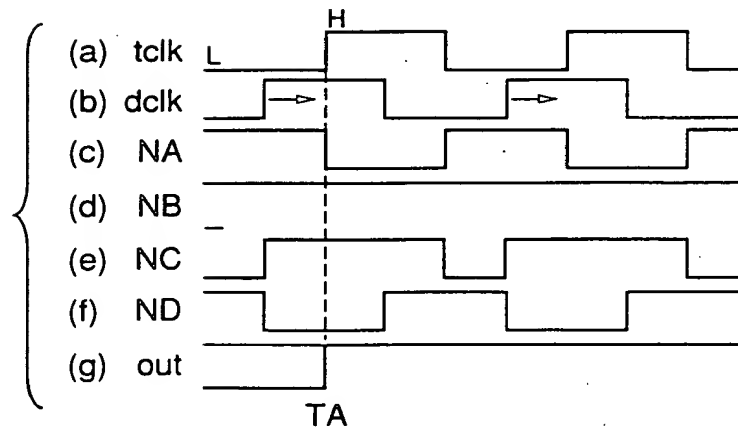


FIG. 11

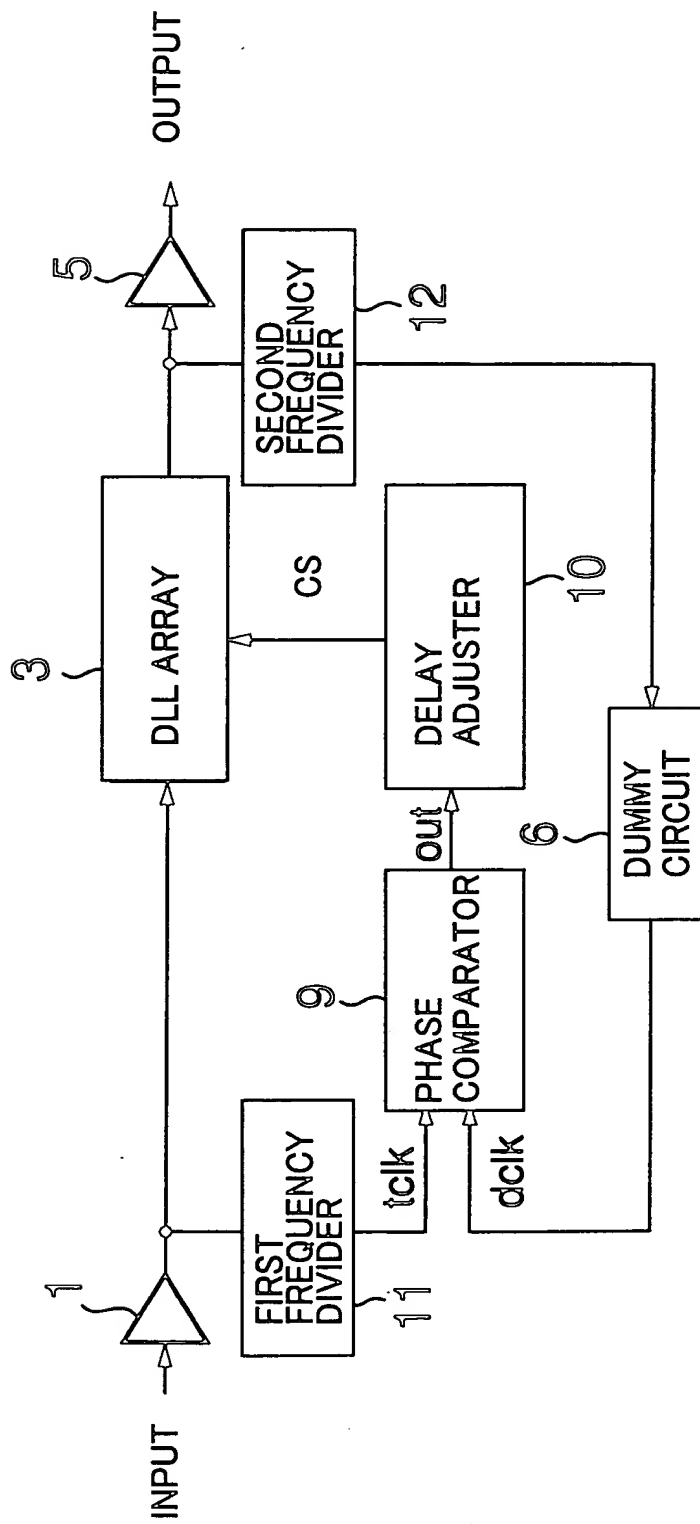
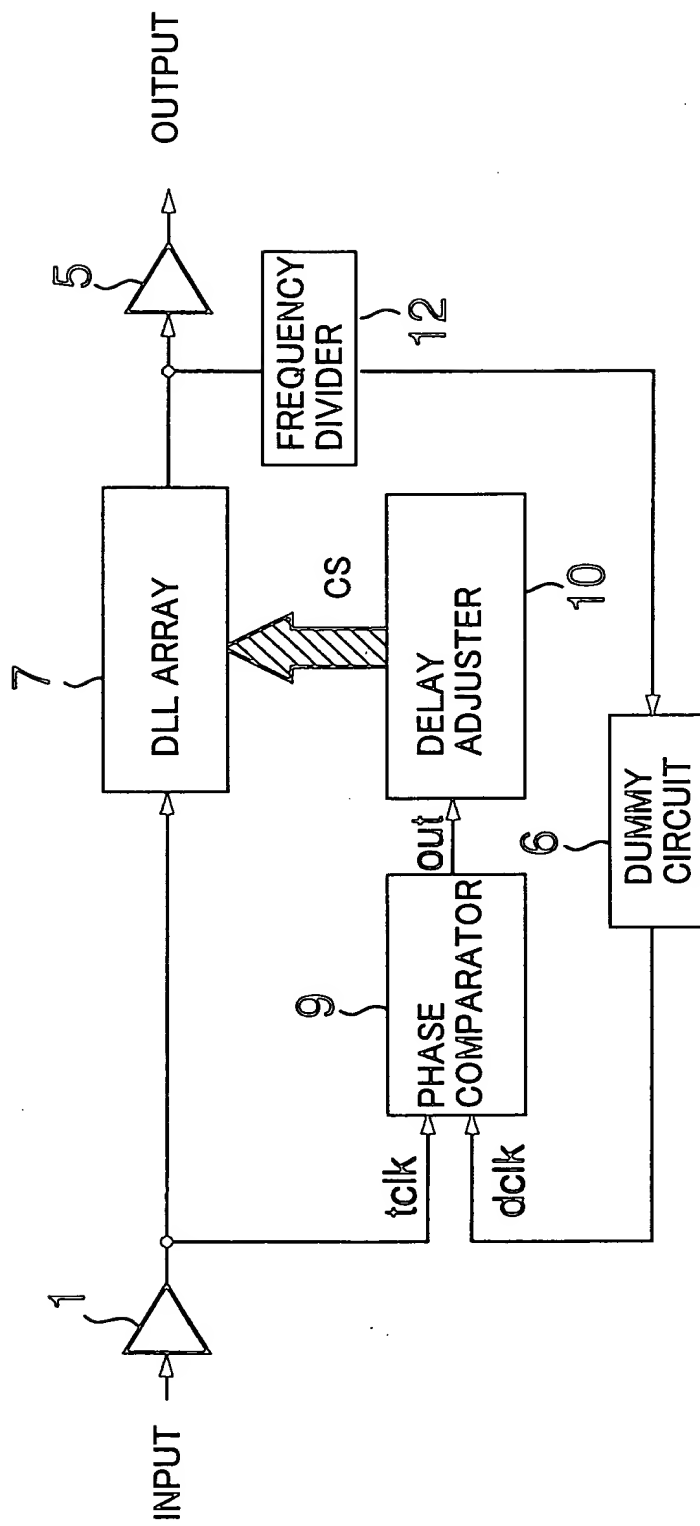


FIG.12



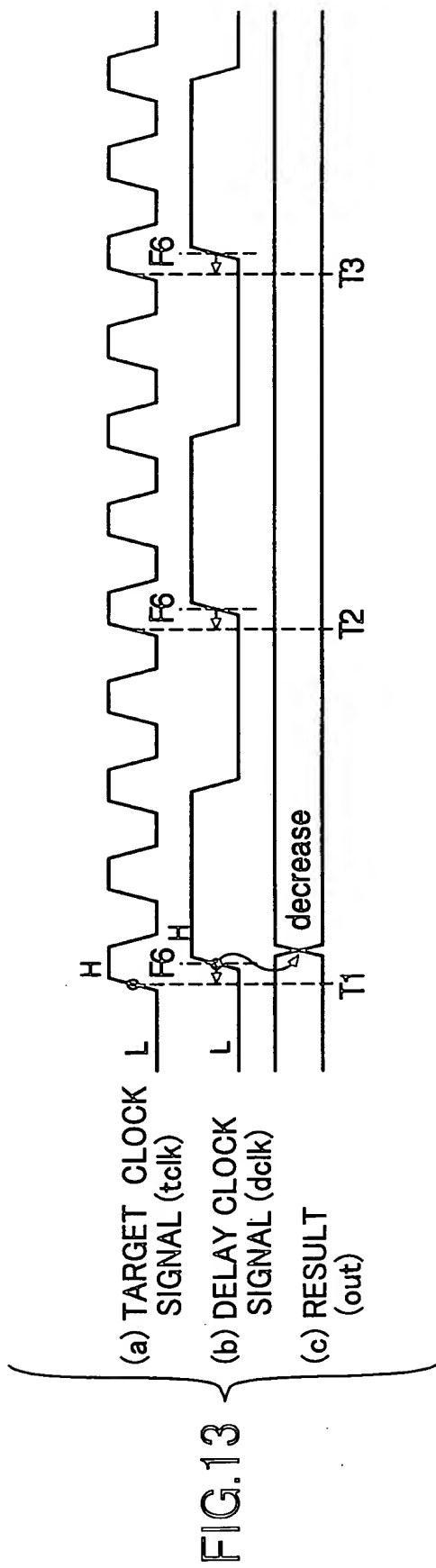
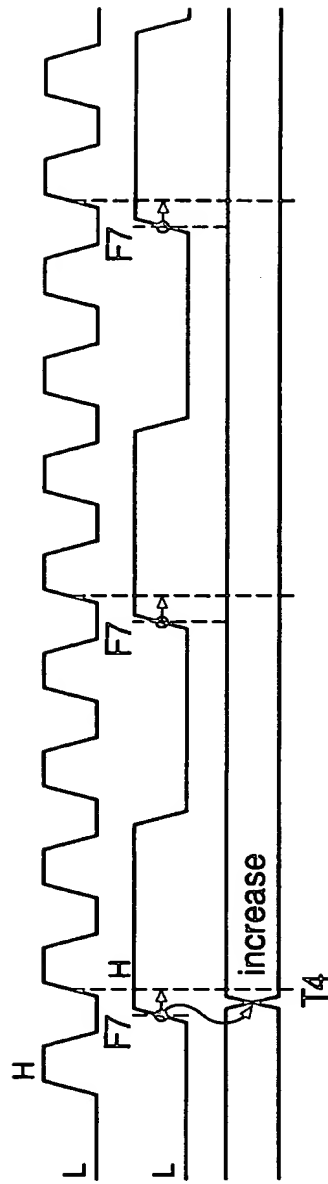


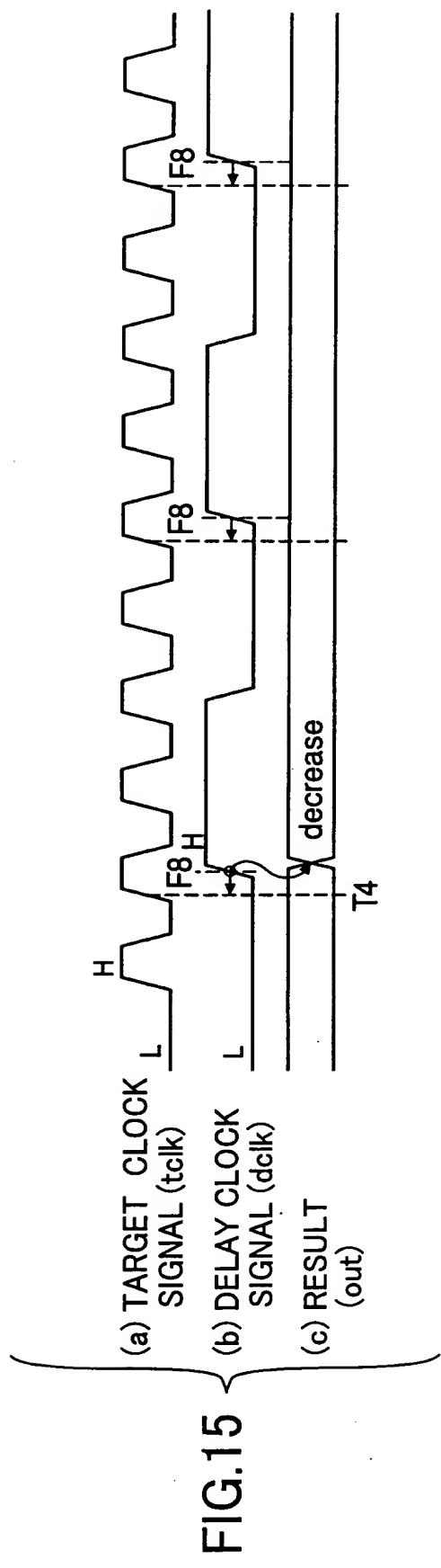
FIG. 14

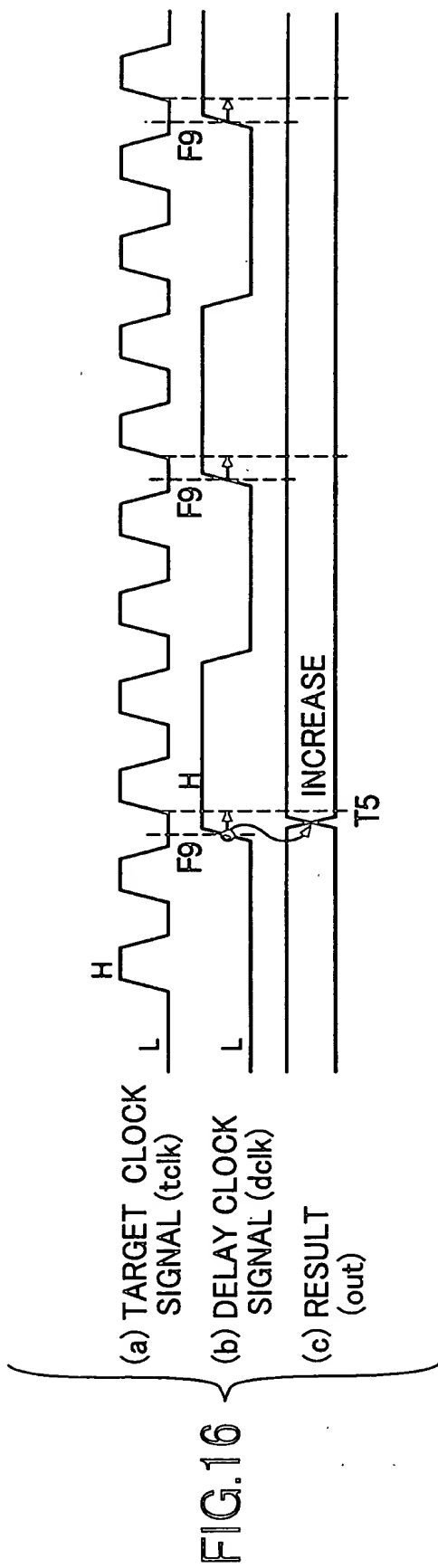
(a) TARGET CLOCK
SIGNAL (tclk)

(b) DELAY CLOCK
SIGNAL (dclk)

(c) RESULT
(out)







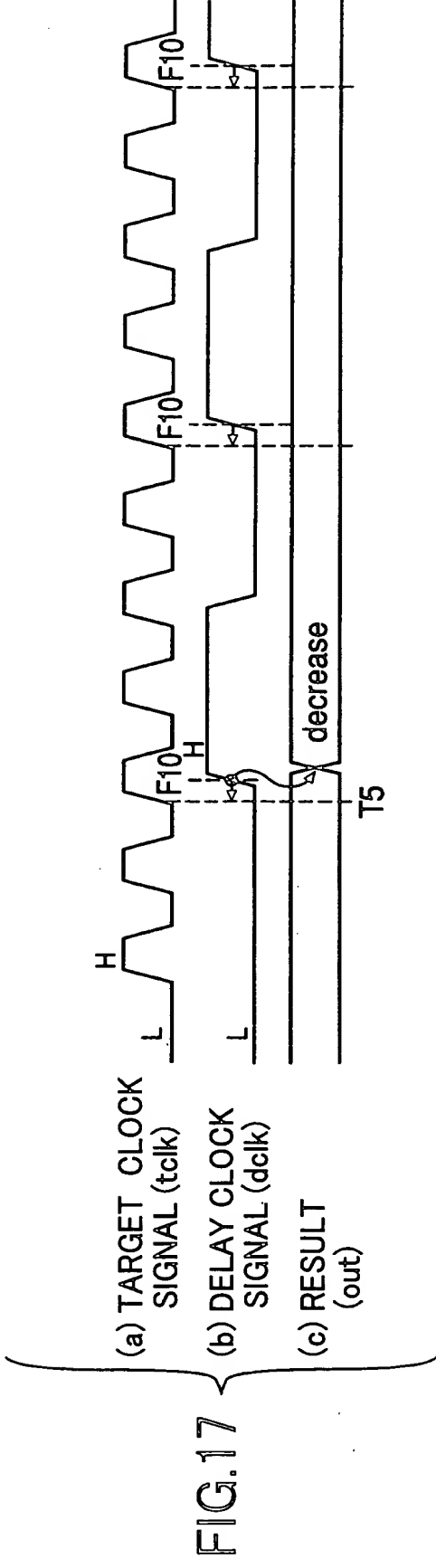


FIG. 18

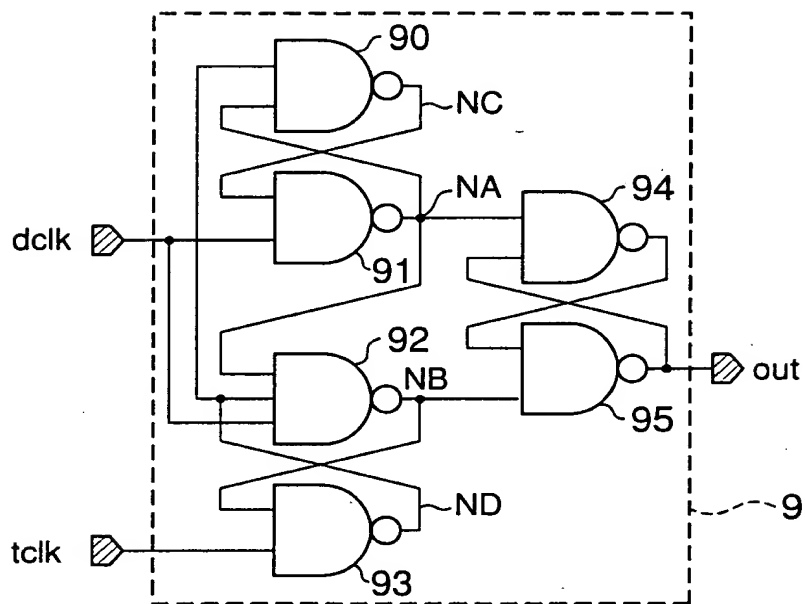


FIG. 19

